IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please maintain the claims in their present form:

1. (previously presented) A digital circuit design verification method comprising:

determining, for each property of a non-reduced RTL model, a reduced RTL model for a design specification by reducing widths of signals occurring in the non-reduced RTL model of the design specification to produce the reduced RTL model retaining the signal property of the non-reduced RTL model; and

subjecting the reduced RTL model to a property checking process.

2. (previously presented) The digital circuit design verification method in accordance with claim 1, further comprising:

determining the design specification and properties of a digital circuit design prior to said determining of the reduced RTL model; and

synthesizing an RTL netlist of high level primitives, so that the digital circuit is defined as an interconnection of control and data path portions where signals of a width n are determined such that $n \in N_+$, wherein N_+ is a positive integer number, and bit vectors of respective lengths each determine a signal value.

3. (previously presented) The digital circuit design verification method in accordance with claim 1,

wherein in the property checking process, an internal bit-level representation contains a bit-level variable for each bit of each word signal, and

wherein said method further comprises sequentially passing the internal bit-level representation to a verification engine and then to a property test unit, to provide a positive result if the property checking holds true and to provide a counter example if the property checking does not hold true.

4. (previously presented) The digital circuit design verification method in accordance with claim 3, further comprising performing signal width enhancement to create a counterexample for the non-reduced RTL model, if the counter example is produced for the reduced RTL model.

5. (previously presented) The digital circuit design verification method in accordance with claim 1,

wherein the non-reduced RTL model includes word-level signals formed of bit-vectors, and

wherein said determining the reduced RTL model is separated into two sequential steps for each bit-vector variable:

computing a coarsest granularity of each word-level signal to separate each word-level signal into several contiguous chunks indicating basic groups of bits with respect to structural data dependencies, and

computing a minimum width with respect to dynamic data dependencies.

6. (previously presented) The digital circuit design verification method in accordance with claim 5, wherein, for each bit-vector variable, said computing of coarse granularities is performed by an equivalence class structure, with an initial satisfiability problem considered as a number of independent satisfiability problems.

7. (previously presented) The digital circuit design verification method in accordance with claim 6, further comprising solving the independent satisfiability problems by bit wise bit-vector functions.

8. (previously presented) A digital circuit design verification tool, comprising:

a pre-property checking unit to reduce widths of signals occurring in a non-reduced RTL model of an input design specification for a digital circuit, to produce a reduced RTL model; and

a verification engine, coupled to the pre-property checking unit, to verify whether signal properties of the non-reduced RTL model hold for the reduced RTL model.

9. (previously presented) The digital circuit design verification tool according to claim 8, further comprising a front end unit, coupled to said pre-property checking unit and to receive input data relating to a design specification and property characteristics of a design to be verified, to provide an RTL netlist of the design specification and property characteristics, so that the digital circuit is defined as an interconnection of control and data path portions, where signals of a width *n* are determined such that $n \in \mathrm{N}_{+}$, wherein N_{+} is a positive integer number, and bit vectors of respective lengths determine signal values.

10. (previously presented) The digital circuit design verification tool in accordance with claim 8,

wherein said pre-property checking unit produces a reduced RTL representation and an internal bit-level representation containing one bit for each bit of each word signal, and

wherein said digital circuit design verification tool further comprises:

a verification engine, coupled to said pre-property checking unit, to receive the internal bit-level representation; and

a property test unit, coupled to said verification engine, to receive the internal bit-level representation, to provide a positive result if a circuit property holds true and to provide a counter example if the circuit property does not hold true.

11. (previously presented) The digital circuit design verification tool in accordance with claim 10, further comprising a signal width enhancement unit, coupled to said property test unit, to receive the counter example for reduced RTL data and to expand the signal width to provide a counter example for the non-reduced RTL model.

12. (previously presented) The digital circuit design verification tool in accordance with claim 8, wherein the non-reduced-width RTL model includes word-level signals formed of bit-vectors, and

wherein said digital circuit design verification tool further comprises:

a coarse granularization unit to determine, for each bit-vector variable, a coarse granularization of each word-level signal and to separate each word-level signal into several contiguous chunks indicating basic groups of bits with respect to structural data dependencies; and

a minimum width determination unit, coupled to said coarse granularization unit, to determine a minimum width with respect to dynamic data dependencies.

13. (previously presented) The digital circuit design verification tool in accordance with claim 12, further comprising an arranging unit, coupled to said minimum width determination unit, to arrange coarse granularities in terms of an equivalence class structure with an initial satisfiability problem considered as a number of independent satisfiability problems.